REMARKS

By the present amendment, independent claims 1, 9, and 21 have been amended, and claims 16-20 have been canceled. Reconsideration and allowance of outstanding claims 1-9, 11-15, and 21-28 in view of the above amendments and following remarks are requested.

The Examiner has rejected claims 1-9 and 11-28 under 35 USC §102(b) as being anticipated by a new reference, U.S. Patent Number 6,615,338 to Tremblay, et al. (hereinafter "Tremblay"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1, 9, and 21, is patentably distinguishable over Tremblay.

Various embodiments according to the present invention relate to an improved performance VLIW processor. Some previous attempts at VLIW processors, such as Tremblay, result in an advantage in parallel processing of a number of instructions. Nevertheless, these VLIW processors exhibit unnecessary power consumption. One reason for such unnecessary power consumption is illustrated with the aid of an example provided by reference to Figure 2 of the present application:

> "After exemplary VLIW packet 200 is fetched from a cache or an external memory, the four instructions in VLIW packet 200 must be forwarded to appropriate execution units for execution. To account for the possibility that all of the instructions in a given VLIW packet may belong to a single issue group, the instruction bus coupled to the execution units of the VLIW processor must be 112 bits wide to carry all four instructions in the VLIW packet at the same time. However, as illustrated in the present example, the first issue group consists of merely two long instructions

> requiring an instruction bus that is only 64 bits wide while the second issue group consists of merely one long instruction and one short instruction requiring an instruction bus that is only 48 bits wide. Thus, in the case of exemplary VLIW packet 200, an instruction bus that is 64 bits wide is all that is needed to handle the processing of both the first and second issue groups in the VLIW packet. As such, a 112-bit wide instruction bus would result in an unnecessary power consumption associated with 48 bus lines that are not needed in the processing of exemplary VLIW packet 200. Further, an instruction bus which is 112 bits wide requires considerably greater chip area as compared with an instruction bus which is only 64 bits wide." See page 4, line 20 to page 5, line 12 of the present application.

As such, conventional VLIW processors have an architectural limitation which not only results in excess power consumption, but also require a relatively large chip area and extra power for instruction buses that are wider than necessary. By reference to Figure 3, internal instruction buses 370 and 380 in the present invention have a width no greater than 64 bits, to handle instruction packets that are 112 bits wide (such as exemplary instruction packets 410 and 430 in the present application). As stated in the present application:

> "[A]ccording to the present embodiment of the invention, the width of each internal instruction bus 370 or 380 does not need to be greater than 64 bits in order to transport the various issue groups to thread A processing unit 303 or thread B processing unit 305 for execution. However, according to conventional VLIW processors, an internal instruction bus having a width of at least 112 bits would be required. The reason is that, according to conventional VLIW processors, it is possible that all of the instructions in a VLIW packet belong to a single issue group. In other words, it is possible that the VLIW packet contains only one issue group. As such, all of the instructions contained in the VLIW packet must be transported simultaneously to a processing unit for execution. Thus, in the above examples, the conventional VLIW processor would need a 112-bit wide internal instruction bus. As is known in the art, power is consumed when each bus line corresponding to a particular bit is charged or discharged. Moreover, and in general, each line in the bus corresponding to

a particular bit consumes some power in each clock cycle even when that particular bus line is not being used to transfer information during that clock cycle." See page 21, lines 1-15 of the present application.

Independent claims of the present invention have been amended to specifically require a busing architecture with internal instruction buses no greater than 64 bits wide for transport of issue groups to each thread of the VLIW processor. In contrast, Tremblay is directed to a VLIW processor containing independent clustered functional units capable of parallel processing of instructions. More particularly, Tremblay is directed to a core processor 100, and media processing units 110 each disclosed as having an instruction cache 210, an instruction aligner 212, an instruction buffer 214, a pipeline control unit 226, a split register file 216, execution units, and a load/store unit 218. The media processing units 110 use execution units for executing instructions. The execution units include three media functional units (MFU) 220 and one general functional unit (GFU) 222. The media functional units 220 are disclosed to be multiple single-instruction-multiple-datapath (MSIMD) media functional units. Each of the media functional units 220 is disclosed as capable of processing parallel 16-bit components. Various parallel 16-bit operations supply the single-instruction-multiple-datapath capability for the processor 100 including add, multiply-add, shift, and compare. See, for example, Figure 3 of Tremblay and column 6, lines 51-67.

However, Tremblay does not disclose or even suggest a busing architecture for reducing the width of instruction buses, as disclosed and claimed by amended independent claims of the present invention. In other words, Tremblay does not disclose

or suggest a busing architecture with internal instruction buses no greater than 64 bits wide for transport of issue groups to each thread of the VLIW processor.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by amended independent claims 1, 9, and 21 is not taught, disclosed, or suggested by the art of record. Thus, amended independent claims 1, 9, and 21 are patentably distinguishable over the art of record. As such, the claims depending from amended independent claims 1, 9, and 21 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim. Thus, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-9, 11-15, and 21-28 remaining in the present application is respectfully requested.

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